Heritage Institute of Technology

M.Tech. in VLSI

(A PROGRAMME UNDER ECE DEPARTMENT)

Curriculum Structure

Release Date: July, 2018:Ver1.0

May,2019:Ver1.1

COURSE STRUCTURE IN

M.Tech. **VLSI**

1st. Year, Semester I

A. Theory								
Sl. No.	**Course Type**	**Code**	**Course Title**	**Contact Hours/Week**				**Credits**
				L	**T**	**P**	**Total**	
1	Professional core 1	**VLSI5101**	Digital VLSI IC Design	3	0	0	3	3
2	Professional core 2	**VLSI5102**	Embedded Systems Design	3	0	0	3	3
3	Professional Elective PE-1	**VLSI5131**	DSP For VLSI System	3	0	0	3	3
		VLSI5132	VLSI IC Fabrication					
4	Professional Elective PE-2	**VLSI5141**	CAD of Digital System	3	0	0	3	3
		VLSI5142	Modelling of VLSI Device					
5	Mgt. Group	**ECEN5103**	Research Methodology and IPR	2	0	0	2	2
6	Audit 1	**DIMA5116**	Disaster Management	2	0	0	2	0
		INCO5117	Constitution of India					
		PDLS5118	Personality Development					
		YOGA5119	Stress Management by Yoga					
		SANS5120	Sanskrit for Technical Knowledge					
Total of Theory				**16**	**0**	**0**	**16**	**14**

B. Practical								
1	Professional Core Lab1	**VLSI5151**	Digital VLSI IC Design Lab	0	0	4	4	2
2	Professional Core Lab2	**VLSI5152**	Embedded Systems Design Lab	0	0	4	4	2
Total of Practical				0	0	8	8	4
Total of Semester				**16**	**0**	**8**	**24**	**18**

1st. Year, Semester II

Sl. No.	Course Type	Code	Course Title	Contact Hours/Week				Credits
				L	T	P	Total	
1	Professional core 3	**VLSI5201**	Analog VLSI IC Design	3	0	0	3	3
2	Professional core 4	**VLSI5202**	VLSI Design, Testing and Verification	3	0	0	3	3
3	Professional Elective PE-3	**VLSI5231**	Memory Technologies	3	0	0	3	3
		VLSI5232	Low Power VLSI Design					
4	Professional Elective PE-4	**VLSI5241**	Advanced VLSI Processor	3	0	0	3	3
		VLSI5242	Advanced Nano Devices					
5		**VLSI5293**	Term Paper and Seminar	0	0	4	4	2
6	Aud 2	Any one subject from Elective3 or Elective4 buckets	Audit Course – 2	2	0	0	2	0
Total of Theory				**14**	**0**	**4**	**18**	**14**

B. Practical								
1	Professional Core Lab3	**VLSI5251**	Analog VLSI IC Design Lab	0	0	4	4	2
2	Professional Core Lab4	**VLSI5252**	VLSI Design, Testing and Verification Lab	0	0	4	4	2
Total of Practical				0	0	8	8	4
Total of Semester				**14**	**0**	**12**	**26**	**18**

2nd. Year, Semester I

A. Theory								
Sl. No.	**Course Type**	**Code**	**Course Title**	**Contact Hours/Week**				**Credits**
				L	**T**	**P**	**Total**	
1	Professional Elective PE-5	**VLSI6131**	Nanomaterials and Nanotechnology	3	0	0	3	3
		VLSI6132	RF IC Design and MEMS					
2	Open Elective	**MATH6121**	Optimization Techniques	3	0	0	3	3
		CSEN6121	Business Analytics					
		AEIE6122	Intelligent Control					
Total of Theory				**6**	**0**	**0**	**6**	**6**

B. Sessional								
1	Dissertation	**VLSI6195**	Dissertation Phase I	0	0	20	20	10
Total of Semester				**6**	**0**	**20**	**26**	**16**

OPEN ELECTIVES TO BE OFFERED BY ECE DEPARTMENT (3rd. Semester):

Open Elective	**ECEN6121**	Ad Hoc Networks and Uses	3	0	0	3	3
	ECEN6122	Design of Embedded Systems					
	ECEN6123	Cognitive Radios					
	ECEN6124	Automation in VLSI Design					

2nd. Year, Semester II

Sl. No.	Course Type	Code	Course Title	Contact Hours/Week				Credits
				L	T	P	Total	
1	Dissertation	**VLSI6295**	Dissertation Phase-II	0	0	32	32	14
2	Grand Viva	**VLSI6297**	Comprehensive Viva Voce	-	-	-	-	2
Total of Semester				**0**	**0**	**32**	**32**	**16**

Total Credit Points = 68

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Release Date: July, 2018:Ver1.0

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M.Tech. - VLSI
Syllabus for First Year

Course Title : Digital VLSI IC Design					
Course Code : VLSI5101					
Contact Hours	**L**	**T**	**P**	**Total**	**Credit Points**
per week	**3**	**0**	**0**	**3**	**3**

CO (Course Outcome):

1. Students will learn CMOS Circuit used in Digital VLSI Domain
2. Students will learn Physical Layout Design of CMOS Standard Cell
3. Students will learn Digital VLSI Design Methodology
4. Students will learn HDL coding
5. Students will learn EDA High Level and Logic Level Synthesis Algorithms
6. Students will learn EDA Physical Place and Route Automation Algorithms

Module I: VLSI Circuits & Physical Layout: [12L]

Unit1: MOS Transistor Characteristics, MOS as Digital Switch, NMOS Logic Family, CMOS Logic Family, CMOS Inverter Characteristics (VTC), Inverter Delay & Noise, NAND and NOR gates, Complex Logic Circuits, Logical Effort, Pass Transistor Logic & Transmission Gate, CMOS Sequential Circuits, CMOS D-Latch and D-Flip-Flop, Pseudo NMOS Logic, Dynamic gate, Domino and NORA Logic

Unit2: CMOS Cross Section, Layout and Mask layers, Inverter Layout, Lambda Rule vs Micron Rule, Std Cell Layout Topology, Stick Diagram, Euler Path Algorithm, Layout Legging.

Module II: VLSI Design Methodology: [8L]

Unit1: Moore's Law, Scale of Integration (SSI, MSI, LSI, VLSI, ULSI, GSI), Technology growth and process Node,

Unit2: Full Custom Design, Std Cell based Semi Custom Design, Gate Array Design, PLD, FPGA: CLB, LUT, MUX, VLSI Design Cycle, Y-Chart.

Module III: EDA Tools: High level Synthesis and HDL: [8L]

Unit1: High level Synthesis EDA Flow, Control and Data Flow Graph, Scheduling, Allocation, Binding, RTL

Unit2: Why HDL ? Frontend Design Flow using HDL (Behavioral, RTL and Gate Level), VHDL/Verilog Modeling: Behavioral, Data-Flow, Structural and Mixed, FSM Example: Mealy Machine and Moore Machine.

Module IV: EDA Tools: Logical Synthesis and Physical Design Automation: [12L]

Unit1: Combinational Logic Optimization: BDD: Binary Decision Diagram, OBDD, ROBDD, Technology Mapping: Pattern DAG, Subject DAG, Sequential Logic Optimization

Unit2: Physical Layout Automation EDA Flow, Partitioning: KL Algorithm, Floor-planning cost function, Placement, Detailed Routing: Channel Routing, Horizontal Constraint Graph, Vertical Constraint Graph, Cyclic Constraint, Left-edge Algorithm, Global Routing: Steiner Tree, Maze Routing.

Text Book:

1. Principles of CMOS VLSI Design, A Systems Perspective, Author: Neil Weste, Kamran Eshraghian, Addison Wesley, 2nd Edition, 2000
2. Algorithms for VLSI Physical Design Automation, Author: N. Sherwani, KLUWER ACADEMIC PUBLISHERS (3rd edition)

Reference Book:

3. CMOS Digital Integrated Circuits, Analysis and Design, Author: Sung-Mo Kang, Yusuf Leblebici, Tata McGraw Hill (3rd Edition), 2006
4. CMOS VLSI Design, A Circuits and Systems Perspective (3rd Edition) Author: Neil Weste, David Harris, Ayan Banerjee. Pearson, 2011
5. Digital Integrated Circuit, Design Perspective, Author: .M. Rabaey, Prentice-Hall
6. VLSI Design and EDA TOOLS, Author: Angsuman Sarkar, Swapnadip De, Chandan Kumar Sarkar, SCITECH PUBLICATIONS (India) Pvt. Ltd., 2011
7. Algorithms for VLSI Design Automation, Author: Gerez, Wiley, 2011
8. A VHDL Primer, J. Bhasker, Prentice-Hall, 2013

Course Title: EMBEDDED SYSTEMS DESIGN					
Course Code : VLSI5102					
Contact Hours	L	T	P	Total	Credit Points
per week	3	0	0	3	3

CO (Course Outcome):

1. Students will learn Embedded System Design Methodology
2. Students will learn Embedded Processor Design
3. Students will learn 8051 Micro-controller
4. Students will learn basics of PIC & ARM Micro-controller
5. Students will learn Embedded Memory Architecture and Interface
6. Students will learn I/O Device configurations and Interfacing

Module I : Introduction to embedded systems: [8L]
Embedded systems overview with various type of examples in different domains such as in communication systems, robotics application and in control application, Design challenge – optimizing design metrics, embedded processor technology, Difference between embedded computer systems and general purpose computer Systems, Design methodology.

Module II: Embedded system processor design: [12L]
Custom single-purpose processors design: using finite state machine model and RTL model. Standard single-purpose processors design: Timers, and watchdog timers, LCD controller. Interfacing of Embedded Processors: Hardware protocol basics, interfacing with a general-purpose processor, RS232, I2C, CAN protocol.

Module III: [10L]
Introduction to 8051 microcontroller: 8051 architecture, pin configuration, I/O ports and Memory organization. Instruction set and basic assembly language programming. Interrupts, Timer/Counter and Serial Communication in 8051, Introduction to PIC & ARM micro-controllers.

Module IV: [10L]
Interfacing with Memory & I/O Devices:
Different types of embedded memory devices and interfacing: SRAM, DRAM, EEPROM, FLASH, CACHE memory. Different types of I/O devices and interfacing: Keypad, LCD, VGA. Square wave and pulse wave generation, LED, A/D converter and D/A Converter interfacing to 8051.

Text Book:
1. Embedded System Design: A Unified Hardware/Software Approach – 2nd Ed Frank Vahid and Tony Givargis

Reference Book:
2. Computers as Components: Principles of Embedded Computing System Design – 2nd Ed Wayne Wolf.

Course Title : DSP for VLSI System					
Course Code : VLSI5131					
Contact Hours	L	T	P	Total	Credit Points
per week	3	0	0	3	3

CO (Course Outcome):

1. Students will learn DSP Algorithm
2. Students will learn Signal and Data flow graph
3. Students will learn Pipelining and Parallel Processing
4. Students will learn Retiming Techniques
5. Students will learn SISO systems
6. Students will learn MIMO Systems

Module I: **DSP Algorithms: [14L]**
Typical DSP Algorithms, Adaptive Filters, Discrete Cosine Transform, Vector Quantization, Viterbi Algorithm, Decimator & Expander, Wavelet Transform, Filter Banks.

Module II: **Iteration Bound: [8L]**
Signal-flow graph, Data-flow graph, Dependence graph, Critical path, Loop & Iteration bounds, Computation of iteration bound .

Module III: **Pipelining and Retiming Techniques: [8L]**
Fine-grain pipelining of FIR filter, Low power aspects for pipelining and parallel processing, Cutset retiming, Clock period and Register minimizations.

Module IV: **Unfolding Algorithms: [10L]**
SISO and MIMO systems, properties of unfolding, sample period reduction, word and bit level parallel processing.

Text Book:

1. VLSI Digital Signal Processing Systems: Design and implementation
   Keshab K Parhi, Wiley India, 2008

Reference Book:

2. DSP Processor Fundamentals: Architectures and Features, Phil Lapsley, Jeff Bier, Amit Shoham, Edward Lee, Wiley – IEEE Press, Jan, 1997
3. Computer Architecture – A Quantitative Approach, John L Hennessy, David A. Patterson,, Elsevier, 2012.

Course Title : VLSI IC Fabrication					
Course Code : VLSI5132					
Contact Hours	**L**	**T**	**P**	**Total**	**Credit Points**
per week	**3**	**0**	**0**	**3**	**3**

CO (Course Outcome):

1. Students will learn Clean Room Concepts.
2. Students will learn individual fabrication steps.
3. Students will learn Pattern Transfer to Si from Mask using Lithography
4. Students will learn Semiconductor Doping Techniques
5. Students will learn planner MOSFET fabrication Process
6. Students will learn SOI fabrication Technology

Module I: Clean Room Technology and Oxidation [12L]

Unit1: Clean room concept- growth of single crystal from melt, surface contamination, cleaning and etching by solvent method and RCA clean.

Unit2: Growth mechanism and kinetics of oxidation, oxidation techniques and systems, oxide properties, oxide induced defects, characterization of oxide films use of thermal oxide and CVD oxide, growth and properties of dry and wet oxides, dopant redistribution, oxide quality. Etching Technology, Different kind of Interconnects, Concept of VIA.

Module II: Diffusion and ion implantation [10L]

Unit1: Diffusion: Fick's equation, atomic diffusion mechanisms, measurement techniques, diffusion in polysilicon and silicon dioxide diffusion systems.

Unit2: Ion Implantation: Range theory, equipments, annealing, shallow junction, high energy implantation.

Module III: Lithography, Deposition and Metallization [12L]:

Unit1: Lithography: Optical lithography, some advanced lithographic techniques

Unit2: Physical vapor deposition: APCVD, Plasma CVD, MOCVD

Unit3: Metallization: different types of metallization, uses and desired properties

Module IV: Process Integration [6L]:

MOSFET technology and MESFET Technology, IC manufacturing, future trends and challenges, SOI fabrication,

Text Book:

1. Semiconductor Devices Physics and Technology, Author: Sze, S.M.; Notes: Wiley, 1985
2. VLSI Technology 2ND Edition, Author: Sze, S.M.; MCGRAW HILL COMPANIES

Reference Book:

3. An Introduction to Semiconductor Microtechnology, Author: Morgan, D.V., and Board, K
4. The National Technology Roadmap for Semiconductors , Notes: Semiconductors Industry Association, SIA, 1994
5. Electrical and Electronic Engineering Series VLSI Technology, Author: Sze, S.M. Notes: Mcgraw-Hill International Editions

Course Title : CAD of Digital System					
Course Code : VLSI5141					
Contact Hours	L	T	P	Total	Credit Points
per week	3	0	0	3	3

CO (Course Outcome):

1. Students will learn graph theory and data structures needed for CAD of VLSI
2. Students will learn basic algorithms needed for CAD of VLSI
3. Students will learn Physical Design Optimization on Partitioning and Floorplan
4. Students will learn Physical Sedign on Place and Route
5. Students will learn High Level and Logic Level Synthesis
6. Students will learn Verilog Modeling

Module I [10L]: VLSI design automation tools – Data structures and basic algorithms, graph theory and computational complexity, tractable and intractable problems.

Module II [10L]: General purpose methods for combinational optimization – partitioning, floor planning and pin assignment, placement, routing.

Module III [10L]: Simulation – logic synthesis, verification, high level Synthesis

Module IV [10L]: MCMS-VHDL-Verilog-implementation of simple circuits using VHDL

Text Book:

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation".

Reference Book:

2. S.H. Gerez, "Algorithms for VLSI Design Automation.

Course Title : Modelling of VLSI Device					
Course Code : VLSI5142					
Contact Hours	**L**	**T**	**P**	**Total**	**Credit Points**
per week	**3**	**0**	**0**	**3**	**3**

CO (Course Outcome):

1. Students will learn BJT Modeling
2. Students will learn MOSFET Operation
3. Students will learn source of various MOSFET Capacitor Components
4. Students will learn SCE (Short Channel Effect) in MOS Devices
5. Students will learn MOS Scaling concepts on Future Technologies
6. Students will learn Industry Standard Compact Modeling

Module I: Semiconductor Physics, p-n junction and BJT [8L]

Semiconductors , Conduction, Contact Potentials, P-N Junction, Modifying the simple diode theory for describing bipolar transistor, Effect of emitter and base series resistances, Effect of base-collector voltage on collector current, Bipolar device models for Circuit and Time-dependent analyses.

Module II: MOS Capacitors and MOSFETs [12L]

Band diagrams for accumulation, depletion and inversion, threshold voltage, weak, moderate and strong inversions, Pao-Sah drain-current model, Source of MOS Capacitance, Transient Response, Capacitance-Voltage curves.

Module III: Scaled MOS Transistors [12L]

Concept of scaling (field, voltage and generalized scaling), ITRS specifications, two-dimensional field patterns and Poisson's equation, charge sharing and barrier lowering, carrier mobility degradation, channel length modulation, velocity saturation, hot carrier effects (gate leakage, impact ionization)

Module IV: Compact Models [8L]

Definitions and types of compact models: physical, empirical and look-up table based models, threshold voltage-based, surface potential-based and charge-based compact models, Commercial compact models.

Text Book:

1. Fundamentals of Modern VLSI Devices by Yuan Taur & Tak H. Ning (Cambridge)

Reference Book:

2. The MOS Transistor (second edition) Yannis Ts ividi s (Oxford)
3. Compact MOSFET Models for VLSI Design by A.B. Bhattacharyya, John Wiley & Sons Pte. Ltd., IEEE Press, 2009.

Course Title: Digital VLSI IC Design Lab					
Course Code : VLSI 5151					
Contact Hours	**L**	**T**	**P**	**Total**	**Credit Points**
per week	**0**	**0**	**4**	**4**	**2**

CO (Course Outcome):

1. Students will learn Cadence Virtuoso
2. Students will learn Schematic Entry of CMOS gates
3. Students will learn Pre layout simulation using Spectra
4. Students will learn Layout Entry of CMOS gates using Nano Technology with key focus on Standard Cells
5. Students will learn Layout Verification Techniques like DRC, LVS, Post Layout Extraction using Assura
6. Students will learn Post layout simulation using Spectra

List of Experiments:

Sub Micron and Deep Sub Micron Technology based Experiments:

1) Introduction to **Cadence Virtuoso & Assura Tools**
    a. Transient, DC, Parametric analysis of CMOS Inverter
    b. Implementation of Various Logic gates using Advanced CMOS technology
    c. Layout design and Verification Using Cadence: Std Cell Layout
    d. Parasitic Extraction, Back-annotation and Post Layout Timing Analysis Using Cadence
2) Introduction to **TCAD Synopsys** Device and Process Simulator: Nano Technology

Course Title: Embedded Systems Design Lab					
Course Code : VLSI5152					
Contact Hours per week	L	T	P	Total	Credit Points
	0	0	4	4	2

CO (Course Outcome):

1. Students will learn Xilinx Vivado Simulator
2. Students will learn VHDL coding and Simulation/Verification
3. Students will learn Finite State Machine coding using HDL
4. Students will learn Test Bench HDL coding for RTL Verification
5. Students will learn FPGA synthesis, Place & Route and Hardware Programming
6. Students will learn ARM Cortex based Software/Hardware

List of Experiments:

1. Introduction to **XILINX-Vivado Simulator, VHDL Coding and Test Bench** Simulation
    a. Logic Design and Verification of a 15 bit Ripple-Carry Adder
    b. Logic Design and Verification of a universal shift register
    c. Logic Design and Verification of a Finite State Moore Machine
    d. Logic Design and Verification of a Finite State Mealy Machine
    e. Design of hand shake protocol to establish Communication between Master and Slave
2. **FPGA Programming Flow** using XILINX Kits: Implementing and verifying many of above experiments in FPGA hardware Kits.
3. **Embedded System Kits**: ARM Cortex M3 Evaluation Board and ARM Cortex based Microcontroller Development Software.
4. **DSP** C6713 Evaluation Kits

Course Title : Research Methodology & IPR					
Course Code : ECEN5103					
Contact Hours per week	**L**	**T**	**P**	**Total**	**Credit Points**
	2	**0**	**0**	**2**	**2**

Research Methodology and IPR

Course Outcome:

At the end of the course, students will be able to

1. Understand research problem formulation
2. Analyze research related information
3. Follow research ethics
4. Understand the ultimate importance of ideas, concept and creativity
5. Importance of IPR for individuals and nations
6. Appreciate that IPR protection provides incentive to inventors for further research work

Syllabus Contents:

Module I [6L]

Meaning of research problem, Sources of research problem, Criteria and characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problems, data collection, analysis, interpretation, necessary instrumentations.

Module II [6L]

Effective literature studies approaches and analysis
Plagiarism, Research ethics

Module III [6L]

Effective technical writing, how to write report, Paper
Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

Module IV [6L]

Nature of Intellectual Property: Patents, Design, Trade and Copyright, Process of Patenting and Development: technological research, innovation, patenting, and development. International Scenario: International cooperation on Intellectual property. Procedure for grants of patents, Patenting under PCT.
Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical indication.
New developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge case studies, IPR and IITs.

References:

- Stuart Melville and Wayne Goddard, "Research and methodology: An introduction for science & engineering students'"
- Wayne Goddard and Stuart Melville, "Research and methodology: An introduction"
- Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
- Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd, 2007
- Mayall, "Industrial Design", McGraw Hill, 1992
- Niebel, "Product Design", McGraw Hill, 1974
- Asimov, "Introduction to Design", Prentice Hall, 1962
- Robert P. Merges, Peter S. Menell, Mark A Lemley, "Intellectual Property in New Technological Age", 2016
- T. Ramappa, "Intellectual Property Rights Under WTO", S Chand, 2008

Course Title : Audit Course 1					
Course Code : DIMA5116					
Contact Hours per week	L	T	P	Total	Credit Points
	2	0	0	2	0

DISASTER MANAGEMENT

Course Outcome: -Students will be able to:
1. learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
2. critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
3. develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
4. critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in.

Syllabus

	Units	CONTENTS	Hours
Module -I	1	**Introduction on Disaster** Disaster: Definition Types of Disaster • Natural Disaster: such as Flood, Cyclone, Earthquakes, Landslides etc. • Man-made Disaster: such as Fire, Industrial Pollution, Nuclear Disaster, Biological Disasters, Accidents (Air, Sea, Rail & Road), Structural failures (Building and Bridge), War & Terrorism etc. • Differences, Nature and Magnitude • Factors Contributing to Disaster Impact and Severity • Repercussions of various types of Disasters o Economic Damage o Loss of Human and Animal Life o Destruction of Ecosystem o Outbreaks of Disease and Epidemics o War and Conflict Natural Disaster-prone areas in INDIA • Areas prone to o Earthquake o Floods and Droughts, o Landslides and Avalanches; o Cyclonic And Coastal Hazards such as Tsunami; Trends of major Disasters and their Impact on India • Lessons Learnt from Recent Disasters	3
	2	**Introduction to Disaster Management** What is Disaster Management	3

		Different Phases of Disasters Disaster Management Cycles Disaster Management Components • Hazard Analysis • Vulnerability Analysis • Prevention and Mitigation • Preparedness • Prediction and Warning • Response • Recovery Disaster Management Act, 2005 National Disaster Management Structure Organizations involved in Disaster Management	
Module -II	1	**Overview on Hazard Analysis and Vulnerability Analysis** **Disaster Preparedness** • Disaster Risk Assessment, People's Participation in Risk Assessment • Disaster Risk Reduction • Preparedness Plans • Community preparedness: Emergency Exercises/ Trainings/Mock Drills	3
	2	**Disaster Prediction and Warning** • Activities o Tracking of disaster o Warning mechanisms o Organizational response o Public education o Communication o Evacuation planning • Current tools and models used for Prediction and Early Warnings of Disaster o Application of Remote Sensing o Data From Meteorological and other agencies o Smartphone/ Web based Apps for Disaster Preparedness and Early Warning used in different parts of Globe	3
Module -III	1	**Disaster Response** • Crisis Management: The Four Emotional Stages of Disaster o Heroic Phase o Honeymoon Phase o Disillusionment Phase o Reconstruction Phase • Need for Coordinated Disaster Response o Search, Rescue, Evacuation, Medical Response and Logistic Management	3

		○ Psychological Response and Management (Trauma, Stress, Rumor and Panic) • Role of Government, International and NGO Bodies	
	2	**Post-disaster Situation Awareness** • Need for Situation Awareness in Post Disaster scenario • Challenges in communication of situational data from affected areas • Need for community-driven disaster management for reliable situation awareness • Crowd-sourcing of situational data: Issues and challenges **Post-disaster Damage and Need Assessment** • Current Trends and Practices – RAPID Damage and Need Assessment • SPHERE standards in Disaster Response • ICT based techniques for Post-disaster damage and need assessment	3
Module -IV	1	**Rehabilitation, Reconstructions and Recovery** • Reconstruction and Rehabilitation as a Means of Development. • Post Disaster effects and Remedial Measures • Creation of Long-term Job Opportunities and • Livelihood Options • Disaster Resistant House Construction • Sanitation and Hygiene • Education and Awareness • Dealing with Victims' Psychology • Long-term Counter Disaster Planning	3
	2	**Disaster Mitigation** • Meaning, Concept and Strategies of Disaster Mitigation • Emerging Trends in Mitigation • Structural Mitigation and Non-Structural Mitigation • Programs of Disaster Mitigation In India	3

SUGGESTED READINGS:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies", New Royal book Company.
2. Sahni, Pardeep et.al. (Eds.)," Disaster Mitigation Experiences And Reflections", Prentice Hall of India, New Delhi.
3. Goel S. L., Disaster Administration And Management Text And Case Studies", Deep & Deep Publication Pvt. Ltd., New Delhi.

Course Name : Sanskrit for Technical Knowledge					
Course Code: SANS5120					
Contact Hours Per Week	**L**	**T**	**P**	**Total**	**Credit Points**
	2	**0**	**0**	**2**	**0**

Course Objectives

1. To get a working knowledge in illustrious Sanskrit, the scientific language in the world
2. Learning of Sanskrit to improve brain functioning
3. Learning of Sanskrit to develop the logic in mathematics, science & other subjects
4. Enhancing the memory power
5. The engineering scholars equipped with Sanskrit will be able to explore the
6. Huge knowledge from ancient literature

Course Outcomes:

After the completion of this course, students should be able to:

1. Understanding basic Sanskrit language
2. Ancient Sanskrit literature about science & technology can be understood
3. Being a logical language will help to develop logic in students

Module I [6L]

- Alphabets in Sanskrit,
- Past/Present/Future Tense,

Module II [6L]

- Simple Sentences
- Order

Module III [6L]

- Introduction of roots
- Technical information about Sanskrit Literature

Module IV [6L]

- Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

References

1. “Abhyaspustakam” – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi
2. “Teach Yourself Sanskrit” Prathama Deeksha-VempatiKutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. “India’s Glorious Scientific Tradition” Suresh Soni, Ocean books (P) Ltd., New Delhi.

Course Name : Personality Development through Life Enlightenment Skills					
Course Code: PDLS5118					
Contact Hours Per Week	**L**	**T**	**P**	**Total**	**Credit Points**
	2	**0**	**0**	**2**	**0**

Course Objectives

1. To learn to achieve the highest goal happily
2. To become a person with stable mind, pleasing personality and determination
3. To awaken wisdom in students

Course Outcomes:

After the completion of this course, students should be able to:

1. Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity
3. Study of Neetishatakam will help in developing versatile personality of students.

Module I [6L]

Neetisatakam-Holistic development of personality

- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride & heroism)
- Verses- 26,28,63,65 (virtue)

Module II [6L]

Approach to day to day work and duties.

- Verses- 52,53,59 (dont's)
- Verses- 71,73,75,78 (do's)
- Shrimad Bhagwad Geeta : Chapter 2-Verses 41, 47,48,

Module III [6L]

Statements of basic knowledge.

- Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35,
- Chapter 18-Verses 45, 46, 48.
- Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68
- Chapter 12 -Verses 13, 14, 15, 16,17, 18

Module IV [6L]

Personality of Role model.

- Shrimad Bhagwad Geeta: Chapter2-Verses 17, Chapter 3-Verses 36,37,42,
- Chapter 4-Verses 18, 38,39
- Chapter18 – Verses 37,38,63

References

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication 2. Department), Kolkata
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.

Course Name : Constitution of India					
Course Code: INCO5117					
Contact Hours Per Week	L	T	P	Total	Credit Points
	2	0	0	2	0

Course Objectives

1. Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
2. To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
3. To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution

Course Outcomes:

After the completion of this course, students should be able to:

1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
2. Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of 1956.

Module I [8L]

- History of Making of the Indian Constitution: History, Drafting Committee, (Composition & Working)
- Philosophy of the Indian Constitution: Preamble, Salient Features

Module II [4L]

- Contours of Constitutional Rights & Duties: Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

Module III [4L]

- Organs of Governance: Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions

Module IV [8L]

- Local Administration: District's Administration head: Role and Importance; Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation; Pachayati raj: Introduction, PRI: ZilaPachayat; Elected officials and their roles; CEO ZilaPachayat: Position and role; Block level: Organizational Hierarchy (Different departments); Village level: Role of Elected and Appointed officials, Importance of grass root democracy
- Election Commission: Election Commission: Role and Functioning; Chief Election Commissioner and Election Commissioners; State Election Commission: Role and Functioning; Institute and Bodies for the welfare of SC/ST/OBC and women.

References

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

Course Name : Stress Management by Yoga					
Course Code: YOGA5119					
Contact Hours Per Week	**L**	**T**	**P**	**Total**	**Credit Points**
	2	**0**	**0**	**2**	**0**

Course Objectives

1.To achieve overall health of body and mind
2.To overcome stress

Course Outcomes:

After the completion of this course, students should be able to:
1.Develop healthy mind in a healthy body thus improving social health also
2.Improve efficiency

Module I [6L]

- Definitions of Eight parts of yog. (Ashtanga)

Module II [6L]

Yam and Niyam.
Do`s and Don't's in life.

- Ahinsa, satya, astheya, bramhacharya and aparigraha
- Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

Module III [6L]

Asan and Pranayam

- Various yog poses and their benefits for mind & body

Module IV [6L]

- Regularization of breathing techniques and its effects-Types of pranayam

References

1. 'Yogic Asanas for Group Tarining-Part-I" :Janardan Swami Yogabhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, AdvaitaAshrama (Publication Department), Kolkata

M.Tech, VLSI, 1st Year 2nd Semester:

Course Title: ANALOG VLSI IC DESIGN					
Course Code : VLSI5201					
Contact Hours	**L**	**T**	**P**	**Total**	**Credit Points**
per week	**3**	**0**	**0**	**3**	**3**

CO (Course Outcome):

1. Students will learn CMOS models for Analog Circuits
2. Students will learn CMOS based Amplifier and OPAMP Circuit components.
3. Students will learn High Frequency (RF) Amplifier Design
4. Students will learn Data Converter (ADC/DAC) Design
5. Students will learn Switched Capacitor Circuits
6. Students will learn PLL/VCO Clock Generator Circuit

Module I: CMOS OPAMP Circuits: [12L]

Unit1: CMOS models for analog circuits - Small signal equivalent circuit, temperature effect and sensitivity, overview of electrical noise. Analog sub-circuits : CMOS switch, resistors, current source, sink, current mirror, voltage and current references.

Unit2: CMOS Amplifiers & CMOS Operation Amplifiers : Basic concepts , Performance Parameters , Single Stage OPAMP, Two stage OPAMP, Stability and Phase compensation, Cascode OPAMP

Unit3: Comparators: Characterisation, Two stage open loop comparators, Discrete time comparators , high speed comparator circuits , CMOS S/H circuits

Module II: RF Analog Circuits & Sub-circuits: **[8L]**

Capacitors and Inductor s in VLSI circuits , Bandwidth estimation techniques, Design of high frequency amplifiers , Design of low noise amplifiers ,Design of Mixers of RF power amplifiers , Architectures of RF receivers and transmitters.

Module III: Data Converter Fundamentals & Architecture: [10L]

Ideal D/A converters, Ideal A/D
converter, Serial and Flash D/A converters and A/D converters, Medium and High Speed converters, Over-sampling converters, performance limitations, Design considerations.

Module IV: Special Circuits: [10L]

Unit1: Switched Capacitor circuits: General considerations, Resistor simulation using different Switched Capacitor topologies, Switched Capacitor integrators, First and second order switched capacitor filter circuits.

Unit2: CMOS voltage controlled oscillators, Phase locked loops, Ring oscillators.

Text Book:

1. CMOS Analog Circuit Design (second edition) Phillip E. Allen and Douglas R. Holberg (Oxford)

Reference Book:

1. The MOS Transistor (second edition) Yannis Tsividi s (Oxford)

Course Title: VLSI Design, Testing and Verification					
Course Code : VLSI5202					
Contact Hours	L	T	P	Total	Credit Points
per week	3	0	0	3	3

CO (Course Outcome):

1. Students will learn embedded Memory Design in VLSI Chip
2. Students will learn VLSI Interconnect Design
3. Students will learn Industry Standard STA (Static Timing Analysis) Method
4. Students will learn Set-up and hold Checks for Timing Verification
5. Students will learn process variation and Clock skew concepts
6. Students will learn Si Testing/Debug Methods

Module I: VLSI Memory Design: [12L]
Types of Memory, Memory Organization, Memory Folding Criteria, Memory Cell Design Method for Write and Read Operation, Critical Path Analysis & Memory Access Time, DRAM 4T, 3T, 1T Cell Design Method, SRAM 8T, 6T Cell Design Method, Sense Amplifier Operation, Multiport Register File Design Challenges, Mask ROM, ROM Programming Techniques, Flash ROM

Module II: VLSI Interconnect Design: [6L]
Component of Interconnect, Interconnect Cross Section, Wire material, Interconnect Modelling, Interconnect Design Issues and WirePlan: Capacitance, Delay, Lumped Model vs Distributed Model, RC Scaling, Repeater, Interconnect Power, Interconnect Noise: Coupling, Cross Talk

Module III: VLSI Verification Flows and Static Timing Analysis: [12L]
Unit1: Logic Verification, Circuit Verification, Layout Verification (DRC, LVS), pre-layout simulation, parasitic Extraction and Back-annotation, post layout verification,
Unit2: Timing checks (set-up, hold), process variation study with PVT analysis, Library Cell characterization, Static Timing Analysis: Types of Path for Timing Analysis, Launch path, Capture Path, Longest Path, Shortest Path, Critical Path, Clock Skew

Module IV: Si-Testing: [10L]
Why Testing, Challenge of Si-Testing, Manufacturing Defects, Die (Inter and Intra) Variation, Yield, DPM, Combinational Circuit Testing: Logical Fault Modelling: Stuck at Faults (D-Algorithm), Bridging Fault, Transistor Stuck open/Stuck Short, ATPG, Path Delay Fault, Sequential Circuit Testing: DFT, Scan Design, SFF, LSSD-SSF, BIST

Text Book:

1. Principles of CMOS VLSI Design, A Systems Perspective, Author: Neil Weste, Kamran Eshraghian, Addison Wesley, 2nd Edition, 2000
2. VLSI Test Principles and Architectures, Design for Testability, Author: Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, The Morgan Kaufmann series in Systems on Silicon. 2006 Elsevier

Reference Book:

1. CMOS VLSI Design, A Circuits and Systems Perspective (3rd Edition) Author: Neil Weste, David Harris, Ayan Banerjee. Pearson, 2011
2. Digital Integrated Circuit, Design Perspective, Author: .M. Rabaey, Prentice-Hall

Course Title : Memory Technologies					
Course Code : VLSI5231					
Contact Hours	**L**	**T**	**P**	**Total**	**Credit Points**
per week	**3**	**0**	**0**	**3**	**3**

CO (Course Outcome):

1. Students will learn SRAM Bit-cell Design
2. Students will learn SRAM architecture and periphery Circuits
3. Students will learn DRAM Bit cell Design
4. Students will learn DRAM architecture, periphery Circuits and Controller
5. Students will learn various ROM Design
6. Students will learn Future Memory Technologies like MRAM, FRAM

Module I: SRAM: [10L]
Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

Module II: DRAM: [10L]
MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs, DRAM Memory controllers.

Module III: Non-Volatile Memories: [10L]
Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

Module IV: Advanced Memory Technologies: [10L]
Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

Text Book:

1. Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and Applications”, Wiley Interscience

Reference Book:

1. Kiyoo Itoh, “VLSI memory chip design”, Springer International Edition
2. Ashok K Sharma,” Semiconductor Memories: Technology, Testing and Reliability , PHI

Course Title : Low Power VLSI Design					
Course Code : VLSI5232					
Contact Hours	**L**	**T**	**P**	**Total**	**Credit Points**
per week	**3**	**0**	**0**	**3**	**3**

CO (Course Outcome):

1. Students will learn source of CMOS Dynamic Power Dissipation
2. Students will learn CMOS Dynamic Power Reduction Techniques
3. Students will learn source of CMOS Standby (leakage) Power Dissipation & Reduction Techniques
4. Students will learn Short Circuit Power Reduction Techniques
5. Students will learn Embedded Memory Power Reduction Techniques
6. Students will learn System and Architecture level Power Reduction Techniques

Module I: Dynamic Power Reduction: [12L]

Unit1: Introduction: Why Low Power ? Definition of dynamic power, Transition probability, Signal probability, Transition probability of basic gates, Glitch power, source of switching capacitance

Unit2: Dynamic Power reduction with Vdd, Delay vs Power Trade-off, Dual Vdd, Dynamic Voltage Scaling (DVS), Dynamic Power Management, Capacitance Scaling, Transistor sizing, Transition probability reduction by clock gating, Logic restructuring, Input Reordering, Glitch reduction

Module II: Standby Power Reduction: [12L]

Unit1: Leakage power definition, Gate Leakage, Channel Leakage, Junction Leakage. Channel leakage issue with Threshold Scaling, Leakage vs Dynamic power

Unit2: Technology Solution of Gate Leakage reduction: High-K, FinFET, Channel leakage reduction techniques: Multiple Threshold Voltage, Long Channel Transistor, Device Downsizing, Stacking, Power Gating, Dual Vdd, Dynamic Body-Biasing, Technology Solution: FinFET

Module III: Short Circuit Power Reduction: [6L]

Definition, Dependency on Load Capacitance, Various reduction techniques

Module IV: Power **Reduction at Various Design Phase: [10L]**

System level, Algorithm level, Architecture Level (Parallel vs Pipeline), Gate level, transistor level, Power Analysis Tool, Low Power Memory Circuit Example on DRAM, SRAM, ROM, Power issue with Dynamic Gates: Floating node and Keeper Solution.

Text Book:

1. Practical Low Power Digital VLSI Design, Author: Gary Yeap, KLUWER ACADEMIC PUBLISHERS, 2010

Reference Book:

1. Low Power CMOS VLSI Circuit Design, Author: Kuashik Roy and Sharat Prasad, John Wiley & Sons, Inc. 2009

Course Title : Advanced VLSI Processor					
Course Code : VLSI5241					
Contact Hours	**L**	**T**	**P**	**Total**	**Credit Points**
per week	**3**	**0**	**0**	**3**	**3**

CO (Course Outcome):

1. Students will learn basic structure of instruction set architecture (ISA)
2. Students will learn CISC and RISC Architecture
3. Students will learn sample DSP Processor Architecture
4. Students will learn Accelerator
5. Students will learn Multi-Threaded Processor
6. Students will learn use of Microprocessor cores in SOC Design

Module I: Fundamentals: [8L]
Architecture organization, basic structure of instruction set architecture (ISA arch) and Flynn's taxonomy. Comparison of Von-Neumann and Harvard architecture, Microcoded and hardwired control architecture, scalar and Vector processors architecture, CISC and RISC architecture. Basic of pipelining, pipeline hazards and solutions

Module II: The DSP and Its Impact on Technology: [12L]
Parallel computation using superscalar architecture, description of the very long Instruction word architecture (VLIW arch) , detail description of TI TMS320C5x DSP processor architecture.

Module III: Accelerator :[10L]
Need for accelerators, Accelerators and different types of parallelism, Processor architectures and different approaches to acceleration. General-Purpose Embedded Processor Cores: The ARM.

Module IV: Multiprocessor and multithreaded processor [10L]
Utilization of course-grain parallelism, chip-multiprocessors, multithreaded processors, SMT processor, A benefits analysis of processor customization, Using microprocessor cores in SOC design, Benefiting from microprocessor extensibility, how microprocessor use differs between SOC and board-level design

Text Book:
1. Computer Architecture: Pipelined and Parallel Processor Design – 2nd Ed Michael J. Flynn

Reference Book:
1. Digital Signal Processors: Architecture, Programming and Applications - B. Venkataramani, M. Bhaskar
2. ARM System-on-Chip Architecture – 2nd Ed Steve Furber
3. Computer System Design: System-on-Chip – 1st. Ed Michael J. Flyn, Wayne Luk

Course Title : Advanced Nano Devices					
Course Code : VLSI5242					
Contact Hours		**T**	**P**	**Total**	**Credit Points**
per week	**3**	**0**	**0**	**3**	**3**

CO (Course Outcome):

1. Students will learn various leakage phenomena in advanced MOS
2. Students will learn High K Plus Metal Gate Technology for advanced Process Nodes
3. Students will learn SOI MOS device
4. Students will learn FinFET Devices like DGMOS, Tri-gate
5. Students will learn Hetero-Structures
6. Students will learn CNT, Graphene Device

Module I: Leakage Current Mechanisms and Reduction (6+6=12L)

Unit 1: Sub-threshold leakage, band-to-band leakage, gate-oxide tunneling, gate-induced-drain leakage etc.
Unit 2: High-K gate dielectric and Metal-gate technology: Concept of EOT, leakage current control, use of various high-K oxides, work function engineering, Fermi-level pinning.

Module II: SOI MOSFETs [6L]

Partially-depleted SOI, Fully-depleted SOI, Advantages and disadvantages of SOI structure.

Module III: Multigate Structures [12L]

DG-MOSFETs, TRI Gate MOSFETs, FinFETs, Surround gate MOSFETs, Omega Gate MOSFETs, Volume inversion, Random Dopant Fluctuation, Concept of undoped body, Underlap device structure, Symmetry and asymmetry MOSFET structure.

Module IV: Hetero Structures and Quantum Well devices [10L]

Quantization and low-dimensional electron gas, band alignment in Si/SiGe hetero-structures, HEMTs, Carbon Nano-tube, Graphene device.

Text Book:

1. The MOS Transistor (second edition) Yannis Tsividis (Oxford)

Reference Book:

1. Fundamentals of Modern VLSI Devices by Yuan Taur & Tak H. Ning (Cambridge)
2. FinFETs and Other Multi-Gate Transistors by J.P. Colinge, Springer, 2008.

Course Title : Analog VLSI IC Design Lab					
Course Code : VLSI5251					
Contact Hours	**L**	**T**	**P**	**Total**	**Credit Points**
per week	**0**	**0**	**4**	**4**	**2**

CO (Course Outcome):

1. Students will learn DC, Transient and AC analysis of Analog Circuits
2. Students will learn MOS based Current Mirror Circuit Design in Cadence Environment
3. Students will learn Design of Single Stage Amplifier using Virtuoso/Spectra
4. Students will learn Design of Differential Amplifier using Virtuoso/Spectra
5. Students will learn ADC/DAC Design in Cadence Environment
6. Students will learn TI based Analog System Lab Starter Kits

List of Experiments:

Sub Micron and Deep Sub Micron Technology based Experiments:

1) **Cadence Virtuoso and Assura Tool** Based Analog Experiments
    a. MOS as Resistors, Current Source, Sink, Current Mirror
    b. DC, Transient and AC analysis of Single Stage Amplifier
    c. Layout Design and Verification of Single Stage Amplifier
    d. Circuit and Layout design of Differential Amplifier
    e. Circuit and Layout design of Operational Amplifier
    f. ADC/DAC Design
2) Introduction to **Texas Instruments Analog System Laboratory Starter Kits** (ASLK)

Course Title : VLSI Design, Testing and Verification Lab					
Course Code : VLSI5252					
Contact Hours	**L**	**T**	**P**	**Total**	**Credit Points**
per week	**0**	**0**	**4**	**4**	**2**

CO (Course Outcome):

1. Students will learn Critical Path Modeling and Analysis
2. Students will learn Sizing in Digital Design
3. Students will learn CMOS Design of Combinational Circuits and Modules
4. Students will learn CMOS Design of Sequential Circuit, Setup and Hold Check
5. Students will learn Layout of a system, DRC, LVS, Extraction using Cadence Virtuoso/Assura
6. Students will learn Back-annotation and Post Layout Timing Analysis using Spectra

List of Experiments:

Sub Micron and Deep Sub Micron Technology based Experiments:

1) Combinational Circuit Example (**Cadence Virtuoso and Assura Tools**)
    a. Circuit Design,
    b. Critical Path Timing Analysis,
    c. Layout Design and Verification,
    d. Parasitic Extraction, Back-annotation and Post Layout Timing Analysis
2) Sequential Circuit Example (**Cadence Virtuoso and Assura Tools**)
    a. Circuit Design,
    b. Setup and Hold Analysis,
    c. Layout Design and Verification,
    d. Parasitic Extraction, Back-annotation and Post Layout Timing Analysis
3) **Cadence Semi Custom Design** Flow
    a. **Incisive Logic Simulation**: Verilog Coding and Test Bench Verification
    b. **Encounter RTL Compiler**: Logic Synthesis
    c. **Encounter Physical Design Implementation**: Floor-planning, Power-planning, Placement, CTS, Routing, Static Timing Analysis
    d. **ASIC views** - .lib, .lef, .gds, .sdf
    e. **Std. cells**- Design, layout, characterization
    f. **Logical Equivalence checking**

M.Tech, VLSI, 2nd Year 1st Semester:

Course Title: Nanomaterials and Nanotechnology					
Course Code : VLSI6131					
Contact Hours	L	T	P	Total	Credit Points
per week	3	0	0	3	3

Course outcomes:

At the end of the course the students would be able to:

1. Understand the basic science behind the design and fabrication of nano-scale systems
2. Gain knowledge regarding the structures of nanomaterials
3. Learn about the preparation of nanoparticles
4. Acquaint themselves with carbon nanotubes and porous materials
5. Understand and formulate engineering solutions for present-day problems and competing technologies for future applications
6. Gather detailed knowledge of the fabrication process.

Module 1: [9L]
Introduction: Introduction to nanomaterials and nanotechnology, top-down and bottom-up methods of synthesis of nanomaterials, self-assembly, Structure of nanomaterials, synthesis of nanoparticles, homogeneous nucleation.

Module 2: [9L]
Preparation of nanoparticles, carbon fullerenes, synthesis of nanowires, nanorods and nanotubes.

Module 3: [9L]
Nanotubes: nanotubes of different materials, carbon nanotubes: graphene, SWNTs, MWNTs, structure of carbon nanotubes, carbon nanotube composite materials, carbon nanotube reactors.

Module 4: [9L]
Porous materials and nano-lithography: classification of pores, synthesis of porous materials, photolithography, soft-lithography, DPN on various materials, toxic effects of nanomaterials.

Books:

1) Introduction to Nanotechnology Paperback – 2007 by Frank Owens Charles Poole – Wiley
2) Nanoscience and Nanotechnology: Fundamentals of Frontiers Paperback – 2013 , Shubra Singh M.S. Ramachandra Rao , Wiley
3) An Introduction to Nanomaterials and Nanoscience (PB) Paperback – 2005 , Das A , CBS Publishers

Course Name: RF IC Design and MEMS					
Course Code : VLSI6132					
Contact Hours per week	**L**	**T**	**P**	**Total**	**Credit Points**
	3	0	0	3	3

COURSE OUTCOMES:

Students should be able to:

1. Specify noise and interference performance metrics like noise figure, IIP3 and different matching criteria.
2. Comprehend different multiple access techniques, wireless standards and various transceiver architectures.
3. Design various constituents' blocks of RF receiver front end.
4. Describe MEMS fabrication technologies.
5. Critically analyze micro-systems technology for technical feasibility as well as practicality.
6. Comprehend the working of various systems and design electronic circuits for various applications.

Module I: [10L]

Prerequisite: RFIC design tradeoffs; Fading,Diversity; Multiple Access Schemes; S and ABCD parameters; Resonance in LC circuit; Concept of transmission lines-Reflection Coefficient; Impedance transformation and matching.

Unit1: RF Devices: Design of RF passive devices- capacitor, inductors; Design of RF MOS devices; Spectre RF ,BJT, MOS spice modeling in RF.

Unit2: RF Systems basics: Nonlinearity in RF Systems; IIP3, SFDR; Classical two port network theory of Noise; Noise in MOSFETs; Testing of RF System – Noise, Distortion Measures and Mitigation Methods.

Module II: [12L]

Unit1: RF System Blocks: Wideband amplifier design; LNA Design; Mixer Design, Gilbert mixer; Linearization techniques; Design Overview of oscillator and Mixer, Frequency Synthesizer; VCO design; power amplifier design – A,B,AB,C,D,E,F;

Unit2: Transmitter Architecture- PLL/CDR Loop, Frequency Divider Unit2: Receiver architectures- direct conversion, heterodyne, image reject architectures; Unit3: Applications- GSM,CDMA architectures.

Module lll: [9L]

Unit1: Introduction to MEMS technology: Basics of MEMS; Areas of application; Silicon as Design material; Important Material Properties and Physical Effects;Other design materials (GaAs,Quartz, SiC, Polymer etc.,)

Unit2: MEMS Fabrication: Bulk micromachining; Surface micromachining; Different types of etchants and etching methods; Nonlithographic Microfabrication Technologies

Module IV: [9L]

Unit1: MEMS Structures and Systems for sensors and actuators: Sensing and Actuation methods; Sensors of different types with example of each type (Mechanical, temperature, chemical , Lab on Chip, microfluidic, bio-sensors);micro pump; 3D Accelerometer, Digital Light Projector

Unit2: MEMS structure and systems for RF applications: Passive Electrical Components: Capacitors and Inductors; Surface-Micromachined Variable Capacitors;Bulk-Micromachined Variable Capacitors ;Micromachined Inductors; Microelectromechanical Resonators; Microelectromechanical Switches

Books:

1)MEMS- Fundamental Technology and Applications, Edited by Vikas Choudhury, CRC Press
2) MEMS Based Circuits and Systems for Wireles Communication, Christian C. Enz, Andreas Kaiser (Editors), Springer
3) RFIC and MMIC design and Technology, Edited by Robertson and S.Lucyzyn, IET publishers

List of Open Electives offered by different Departments
M Tech, Second Year, Semester III

A. Theory							
Department	**Course Code**	**Course Name**	**Scheme Of Studies Per Week**				
			L	**T**	**P**	**Total**	**Credits**
AEIE	**AEIE6121**	**Biosignal and Biomedical Image Processing**	**3**	**0**	**0**	**3**	**3**
	AEIE6122	**Intelligent Control**					
BT	**BIOT6121**	**Engineering Mathematics and Biostatistics**					
ChE	**REEN6121**	**Composite Material for Renewable**					
	REEN6122	**Energy Safety and Hazards in Energy Industry**					
CSE	**CSEN6121**	**Business Analytics**					
	CSEN6122	**Advanced Artificial Intelligence**					
ECE	**ECEN6121**	**AD HOC Networks and Uses**					
	ECEN6122	**Design of Embedded Systems**					
	ECEN6123	**Cognitive Radios**					
	ECEN6124	**Automation in VLSI Design**					
IT	**INFO6123**	**Information Theory and Coding**					
MATH	**MATH6121**	**Optimization Techniques**					